AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An input circuit comprising:

a current mirror circuit including a self-biased transistor and a non-self-biased transistor connected to each other;

a differential circuit including a first transistor a first drain of which is connected to the non-self-biased transistor for receiving an external signal and a second transistor a second drain of which is connected to the self-biased transistor for receiving a reference signal, wherein a first source of the first transistor and a second source of the second transistor are connected in common and have the same potential, and the differential circuit generates a node signal having a rising edge and a falling edge at the first drain in accordance with a current flowing through the first and second transistors;

a constant current source connected to the first source of the first transistor; and

a current regulating circuit connected to the second source of the second transistor and connected in parallel to the constant current source, wherein the current regulating circuit conditions an amount of the current flowing through the differential circuit to be increased in response to the node signal when the first transistor changes its state from an activated state to a deactivated state in response to the external signal and the node signal rises, such that only a rising delay time of the node signal is shortened.

2. (Previously Presented) The input circuit according to claim 1, wherein the external signal has a first transition point and second transition point, wherein the node signal has a third transition point and a fourth transition point corresponding to the first transit point and the second transit point, respectively, and wherein the current

regulating circuit regulates the amount of current flowing through the differential circuit such that a delay time between the first transition point and the third transition point is substantially the same as the delay time between the second and fourth transition points.

3. (Cancelled)

4. (Previously Presented) The input circuit according to claim 1, wherein the constant current source is connected to a high potential power supply, and wherein the current regulating circuit includes a third transistor connected in parallel to the constant current source, the third transistor going ON and OFF in response to the node signal.

5. (Previously Presented) The input circuit according to claim 1, wherein the constant current source is connected to a low potential power supply, and wherein the current regulating circuit includes a third transistor connected in parallel to the constant current source, the third transistor going ON and OFF in response to the node signal.

6. (Currently Amended) A semiconductor integrated circuit comprising:

a plurality of input circuits, each input circuit including:

a differential circuit including a first transistor for receiving an external signal and a second transistor for receiving a reference signal, wherein sources of the first and second transistors are connected in common, and the differential circuit generates a node signal having a rising edge and a failing edge at a drain of the first transistor in accordance with a current flowing through the first and second transistors; and

a current regulating circuit, connected to the differential circuit, which conditions an amount of the current flowing through the differential circuit to be increased in response to the node signal when the first transistor changes its state from an activated

state to a deactivated state in response to the external signal and the node signal rises, such that only a rising delay time of the node signal is shortened;

a plurality of complementary signal generating circuits, each connected to one of the input circuits, wherein the complementary signal generating circuits receive the node signal from the associated input circuit and generate a complementary signal of the input signal; and

a plurality of signal processing circuits connected to the plurality of complementary signal generating circuits, respectively, wherein the signal processing circuits perform predetermined signal processing operations in accordance with the complementary signal.

7. (Original) The integrated circuit according to claim 6, wherein each complementary signal generating circuit includes a plurality of inverter circuits.

8. (Original) The integrated circuit according to claim 7, wherein each complementary signal generating circuit includes the same number of the inverter circuits.

9. (Original) The integrated circuit according to claim 7, wherein the complementary signal has a transition period, and wherein each inverter circuit includes a pair of MOS transistors having a response rate set such that the transition period of the generated complementary signal is constant.

10. (Original) The integrated circuit according to claim 7, wherein the complementary signals each having a rising edge, include a normal phase signal and an inverted phase signal, and wherein each inverter circuit includes a pair of MOS transistors having a response rate set such that the delay time from an edge of the

external signal to the rising edge of the normal phase signal and a delay time from an edge of the external signal to the rising edge of the inverted phase signal is substantially the same.

11. (Original) The integrated circuit according to claim 6, wherein the plurality of input circuits includes:

a first input circuit for receiving an external strobe signal and generating a strobe signal; and

a second input circuit for receiving an external data signal and generating a data signal;

wherein the plurality of complementary signal generating circuits includes:

a first complementary signal generating circuit for receiving the strobe signal and generating a normal phase strobe signal and an inverted phase strobe signal; and

a second complementary signal generating circuit for receiving the data signal and generating a normal phase data signal and an inverted phase data signal; and

wherein the plurality of signal processing circuits includes:

a first latch circuit for latching the normal phase data signal from the second complementary signal generating circuit in accordance with the normal phase strobe signal from the first complementary signal generating circuit; an

a second latch circuit for latching the inverted phase data signal from the second complementary signal generating circuit in accordance with the inverted phase strobe signal from the first complementary signal generating circuit.

12. (Previously Presented) The integrated circuit according to claim 6, wherein the external signal has a first transition point and a second transition point,

wherein the node signal has a third transition point and a fourth transition point corresponding to the first transition point and the second transition point, respectively, and wherein the current regulating circuit regulates the amount of current flowing through the differential circuit such that a delay time between the first transition point and the third transition point is substantially the same as the delay time between the second and fourth transition points.

13. (Original) The input circuit according to claim 12, wherein the differential circuit includes a constant current source connected in parallel to the current regulating circuit.

14. (Previously Presented) The input circuit according to claim 13, wherein the constant current source is connected to a high potential power supply, and wherein the current regulating circuit includes a transistor connected in parallel to the constant current source, the transistor going ON and OFF in response to the node signal.

15. (Previously Presented) The input circuit according to claim 13, wherein the constant current source is connected to a low potential power supply, and wherein the current regulating circuit includes a transistor connected in parallel to the constant current source, the transistor going ON and OFF in response to the node signal.

16. (Currently Amended) An input circuit comprising:

a first MOS transistor having a gate that receives a data signal;

a second MOS transistor having a gate connected to a reference voltage, wherein the source of the first transistor is connected to the source of the second transistor at a first node;

a third MOS transistor connected between the first node and a low potential power supply, and having its gate connected to a high potential power supply;

a fourth MOS transistor connected between the first node and the low potential power supply;

a fifth MOS transistor connected between the drain of the first transistor and the high potential power supply;

a sixth MOS transistor connected between the drain of the second transistor and the high potential power supply, wherein the gates of the fifth and sixth transistors are connected to each other and to the drain of the sixth transistor; and

a first inverter having an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor, a node signal having a rising edge and a falling edge is generated at the second node in accordance with a current flowing through the first and second transistors, and wherein the fourth transistor operates to condition an amount of the current flowing through the second transistor to be increased in response to the node signal when the first MOS transistor changes its state from an activated state to a deactivated state in response to the data signal and the node signal rises, such that only a rising delay time of the node signal is shortened.

17. (Original) The input circuit of claim 16, wherein the first, second, third and fourth transistors are NMOS transistors.

18. (Original) The input circuit of claim 17, wherein the fifth and sixth transistors are PMOS transistors.

19. (Original) The input circuit of claim 16, further comprising:

a latch circuit connected to the output terminal of the first inverter.

20. (Original) The input circuit of claim 16, further comprising:

a seventh transistor, connected between the fifth transistor and the high potential power supply, having a gate connected to the low potential power supply;

an eighth transistor connected between the sixth transistor and the high potential power supply, wherein the sources of the fifth and sixth transistors are connected to each other at a third node; and

a second inverter having an input terminal connected to the output terminal of the first inverter and an output terminal connected to the gate of the eighth transistor.

21. (Currently Amended) A semiconductor integrated circuit for receiving a data signal in response to rising and falling edges of a data strobe signal, comprising:

a data strobe signal input circuit which receives the data strobe signal, wherein the data strobe signal input circuit includes:

a differential circuit having a first transistor and a second transistor to generate a differential output signal having a logic level, a first gate of the first transistor receiving the data strobe signal, a second gate of the second transistor receiving a reference signal, and sources of the first and second transistor being connected in common and having the same potential,

a current mirror circuit supplying a current to the differential circuit,

a constant current source coupled to the sources of the first and second transistors, and

a current adjustment transistor coupled to the sources of the first and second transistors, a third gate of the current adjustment transistor receiving the differential

output signal of the differential circuit, wherein the current adjustment transistor operates to condition an amount of the current flowing through the differential circuit to be increased in response to the logic level of the differential output signal when the first transistor changes its state from an activated state to a deactivated state in response to the data strobe signal and the differential output signal rises, such that a rising delay time of the logic level of the differential output signal is shortened.